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# Implementation of ADC in VLSI using AF-PWM

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***Abstract---*** *An integral part of sensor and potential applications is an analog to digital converter (ADCs). The realization of ADC by using "Pulse Width Modulation (PWM)" has been discussed in this work. A reference signal is required by this technique for comparing sampled input signal in analog format for generating "pulse width modulated signals". This ADC offers an advantage of extension to multiple sampling simultaneously. A cheap system based on microcontroller is built by this application. These designs are also characterised by low latency and fast response which makes them useful in biomedical applications in measuring single or multiple inputs.*

***Index Terms---*** *PWM, ADC, Duty cycle, Project Navigator, Modelsim ISE.*

## I. INTRODUCTION

Any real time signal processing system has analog to digital conversion as the most inevitable parts where processing of data is done by computer software such as audio [1][2], and other applications related to sensors [3]. This paper presents an architecture of ADC based on "Pulse Width Modulation" or "Pulse Delay Modulation". The applications of PWM has been found in areas of "pulse coded modulation [4]", and the microcontrollers are used in controlling speed of a step motor [5]. This technique is powerful where variation of duty cycle of a square wave is done for achieving various functionality in above mentioned applications. Devices implemented in medical technology require combination of signal conditioning that includes filtering, amplifier, an ADC and a reference filtering for resolving sensor's signal. Not only small size but the ability of analog circuit to read output of a sensor should have low power for providing prolonged battery life and leads to larger number of readings in smaller time. A widespread popularity has been gained by small and low power consuming devices of medical industry because of small and faster available analogue ICs[6]. The pulse modulation is characterized in two different categories. One method is a "Pulse Width Modulation (PWM)", which finds applications widely such as "switch-mode power supplies (SMPS)". The cycle time of PWM is fixed but there is a variation in duty cycle based on the amplitude of an input signal. The value of pulse width is small for input amplitude of smaller values while it has a large value for larger amplitudes. The "pulse width modulator (PWM)" of analog or digital type is used for realizing such type of signal conversion. The density of pulse is varied based on amplitude of input signal for pulse modulation. This technique has every sample at modulator clock rate sample as a single pulse. The signals of large amplitude are converted and produces a result of large number



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of samples that are at "high" state whereas signals having low amplitudes are met at a "low" state. There is no set time of cycle of this conversion of pulse but a pulse frequency is varied. The sampling of audio signal requires two categories of PWM: "naturally sampled PWM (NPWM) and uniformly sampled PWM (UPWM)". The comparison of low power signal (analog audio) is done with a carrier for creating NPWM in analog PWM modulator. Based on the type of modulation that is, single sided or double sided, a carrier signal is chosen either of sawtooth or triangle respectively. It is beneficial to use a PWM of three levels because it leads to the increase in full bridge configuration's efficiency but also complicating the control.

## II. ANALOG TO DIGITAL CONVERTER

A device for conversion of a "time varying continuous analog signal to a stream of zeros and ones for digitally processing it either by a digital signal processor or a digital computer. The inputs taken by ADCs [7] are input signal, reference signal and a clock signal. Figure 1 illustrates a block diagram.

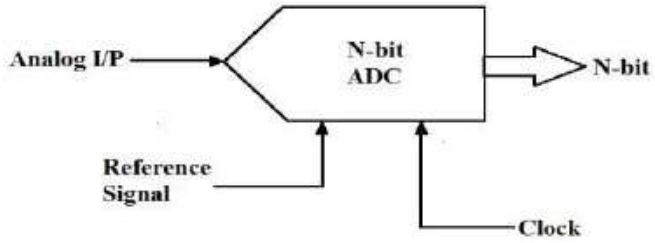


**Fig. 1** Block diagram of ADC (N-bit)

## III. IMPLEMENTATION

This paper presents the implementation of an 8-bit converter capable for conversion of an input analog signal into an 8-bits streams for generating after time Tref of a reference signal.

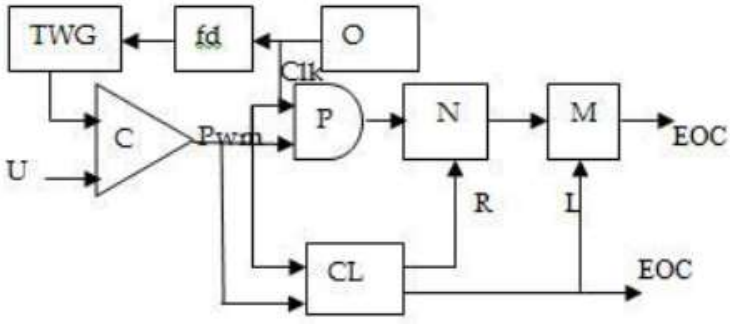


**Fig. 2** Proposed block diagram of PWM ADC

The basic idea in the implementation of analog to digital converter is the conversion of an input signal into a PWM [8] signal. This is done by using a signal generator (triangular) and a comparator as illustrated in figure 2. The division



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is done with 2n of a clock signal that comes from an oscillator O. Here, n is the bit number in a converter. A triangular signal (TWG) is generated by using a divided signal. This is done for comparison of input signal for obtaining a PWM signal[9]. The output of a comparator is low as long as the input signal lies under a triangular signal whereas it goes high when above. When clock signal lies on another input of AND (P) then PWM is a gate signal. When the output is a comparator is high then counter (N) will count after the signal passes gate. The final result of conversion is represented at end of PWM signal's high state. Two signals are generated by a control logic block (CL) based on PWM and clock signals: "Load signal for storing data in the memory latch (M) and Reset signal for clearing the counter for the next measurement". The frequency of a triangle wave gives a "sampling rate"[10]. A PWM signal's duty cycle is computed as given below

$$\frac{A+U_X}{2A} = \frac{\frac{T_X}{2}}{\frac{T_{TW}}{2}}$$

$$T_X = \left\{ \frac{T_{TW}}{2\left(1+\frac{U_X}{A}\right)} \right\} \quad (1)$$

The amplitude of a triangle signal is represented by A, the value of unknown input is denoted by Ux and the period of triangular signal is represented by TTW and high state period is represented by TX. The above equation can be reduced to

$$T_X = 2^n \frac{T_0}{2} \frac{1+U_X}{A} \quad (2)$$

$N_X$ is the total count number that are stored after $T_X$:

$$N_X = T_X/T_O \quad (3)$$

Equation 2 and 3 gives:

$$N_X = 2^{n-1} \frac{1+U_X}{A} \quad (4)$$

The result as shown by equation 4 is displaced binary code. Thus, we get 0 when an input voltage is equal to –A and 0 2n-1 is obtained when input is 0 and 2n is obtained when input is A.

## IV. ALIASING FREE PWM

An amplitude signal a[n] ∈ [0,1] is transformed into a different width stream of two level pulses y[n] having a fixed period of pulse Tp by a digital PWM. The amplitude of a[n] has information in it which is encoded in pulses width y[n]. Asymmetrical pulses around centre of pulse period Tp comprised in pulse train y[n] is a widely used method of asymmetric double edge PWM. The pulse edges and transitions between levels 0 and 1 are determined after finding



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joining point of "amplitude signal a[n] and a triangular reference wave r[n]". Certain constraints should be fulfilled by a[n] for PWM method. There should be a smaller value of bandwidth of a[n] than a reference frequency fp=1/Tp. The value of amplitudes a[n] should fall within the interval ranging between [0,1]. Appropriate steps of pre-processing should be applied to asymmetric double edge PWM. The problem could be solved by adding bias and proper scaling for a signal of real value. PWM is done on signal's magnitude and subsequently phase modulation is applied[11]. A signal combiner is required after performing PWM separately on imaginary and real parts of a signal. The PWM operator which is free from aliasing is

$P$ (a[n], r[n]) is

$$P(a[n], r[n]) = \begin{cases} 1, for\ a[n] \geq r[n] \\ 0, for\ a[n] < r[n] \end{cases} \quad (5)$$

The PWM signal y[n] free from aliasing is given as below:

$$y[n] = a[n] + \sum_{k=1}^{\infty} \frac{2(-1)^k}{\prod k} \sin\left(\prod ka[n]) \cos(2 \prod k \frac{T_s}{T_p} n\right) \quad (6)$$

$T_s$ denotes the time period of the system.

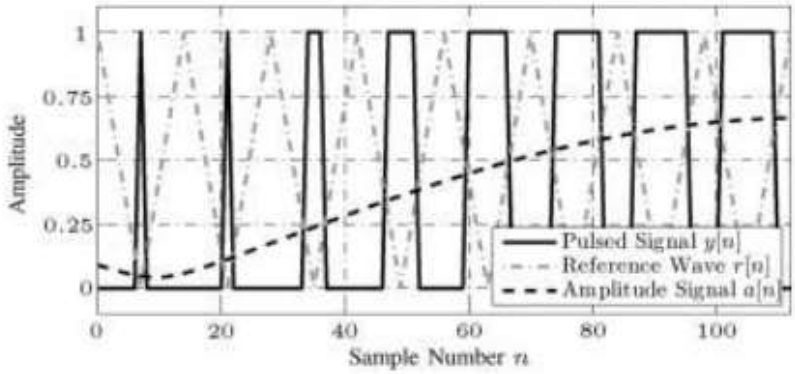


**Fig. 3** PWM signal y[n]

## V. MODELLING IN PROJECT NAVIGATOR

A user friendly software which eases the complicated protocols of communication is Modelsim which are otherwise difficult to carry out. An interactive tool for implementing and synthesizing a design in particular device



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and family. The output is seen in the format of a waveform by designing a model in Xilinx project simulator and Modelsim[12].

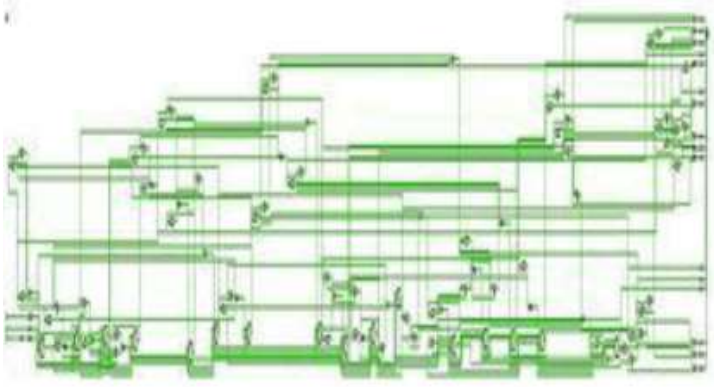

**Fig. 4** Schematic Diagram

The amplitude of reference signal is equal to input signal whereas frequency of input signal is 1 MHz and reference signal is 50 MHz, both being sinusoidal signal. A PWM signal is generated by comparing both signals with each other and generating a stream of 0s and 1s with varying duration[13]. This PWM signal behaves as gate signal to incoming clock signal at a frequency of 126.9 MHz and in the form of a clock signal, final output is fed to a counter with maximum count of 32. After every time period, counter is reset in order to get a digital code for every sample. A positive edge detector is used for detecting rising edge of digitized signal for resetting the value of count after a reference clock's time period[14].

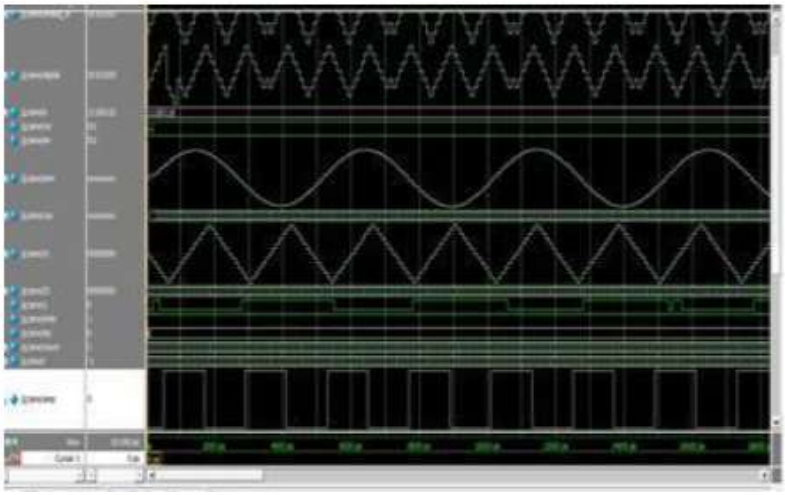

**Fig. 5** RTL Schematic

Thus, it is seen that the shape of digital output waveform is similar to an input signal. The peaks of these triangular waveforms are joined for getting an input signal's waveform. It leads to the digitization of input waveform and



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conversion into a digital code[6]. The digitization of corresponding PWM free from aliasing is shown in figure 6. Figure 5 illustrates a RTL diagram at a frequency of 126.9 MHz.

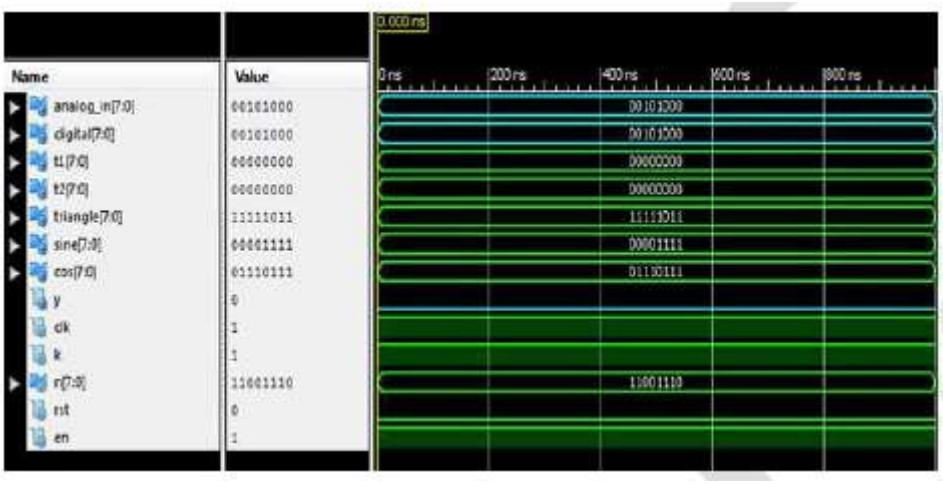


**Fig. 6** Waveform of PWM free from aliasing (ADC)

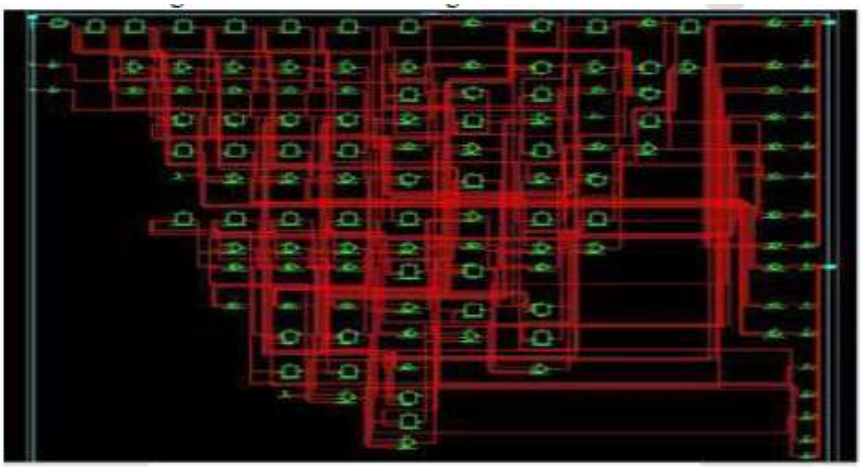

**Fig. 7** Testbench of AF-PWM

The value of inputs are "clk=1, rst=0, en=1, k=1, n(7:0)=11001110" are applied to a circuit. The value of digital output and analog input are same which shows the conversion of ADC without any quantization error.

Table I Area, Power and Delay in PWM

| BLOCK | AREA (cells) | POWER (mW) | DELAY (ns) |
|---|---|---|---|
| PWM based ADC | 2.49 | 0.153 | 7.880 |



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| Device Utilization Summary | | | | |
|---|---|---|---|---|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of Slice Flip Flops | 180 | 1,536 | 11% | |
| Number of 4 input LUTs | 179 | 1,536 | 11% | |
| Number of occupied Slices | 140 | 768 | 18% | |
| Number of Slices containing only related logic | 140 | 140 | 100% | |
| Number of Slices containing unrelated logic | 0 | 140 | 0% | |
| Total Number of 4 input LUTs | 210 | 1,536 | 13% | |
| Number used as logic | 179 | | | |
| Number used as a route-thru | 31 | | | |
| Number of bonded IOBs | 84 | 124 | 67% | |
| Number of BUFGMUXs | 1 | 8 | 12% | |
| Average Fanout of Non-Clock Nets | 2.49 | | | |

**Fig. 8** Reports of area after realization

**Fig. 9** Reports of power after realization



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Destination Clock: clk rising

Data Path: an_0 to cosr_7
                              Gate     Net
  Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FDCE:C->Q             2   0.720    1.216  an_0 (an_0)
   LUT2:I0->O            1   0.551    0.000  Madd_sine_lut<0> (Madd_sine_lut<0>)
   MUXCY:S->O            1   0.500    0.000  Madd_sine_cy<0> (Madd_sine_cy<0>)
   MUXCY:CI->O           1   0.064    0.000  Madd_sine_cy<1> (Madd_sine_cy<1>)
   MUXCY:CI->O           1   0.064    0.000  Madd_sine_cy<2> (Madd_sine_cy<2>)
   MUXCY:CI->O           1   0.064    0.000  Madd_sine_cy<3> (Madd_sine_cy<3>)
   MUXCY:CI->O           1   0.064    0.000  Madd_sine_cy<4> (Madd_sine_cy<4>)
   MUXCY:CI->O           1   0.064    0.000  Madd_sine_cy<5> (Madd_sine_cy<5>)
   MUXCY:CI->O           0   0.064    0.000  Madd_sine_cy<6> (Madd_sine_cy<6>)
   XORCY:CI->O           9   0.904    1.319  Madd_sine_xor<7> (sine_7_OBUF)
   LUT2:I1->O            1   0.551    0.000  Maccum_cosr_lut<4> (Maccum_cosr_lut<4>)
   MUXCY:S->O            1   0.500    0.000  Maccum_cosr_cy<4> (Maccum_cosr_cy<4>)
   MUXCY:CI->O           1   0.064    0.000  Maccum_cosr_cy<5> (Maccum_cosr_cy<5>)
   MUXCY:CI->O           0   0.064    0.000  Maccum_cosr_cy<6> (Maccum_cosr_cy<6>)
   XORCY:CI->O           1   0.904    0.000  Maccum_cosr_xor<7> (Result<7>)
   FDCE:D                    0.203           cosr_7
  ----------------------------------------
  Total                      7.100ns (5.345ns logic, 2.535ns route)
                                     (67.8% logic, 32.2% route)
```

**Fig. 10** Reports of delay after realization

The comparison of performance result is done and denoted in a table form. The table includes delay, power consumption and area of ADC based on AF PWM. The context of "Analog to Digital conversion" is represented by output format by using a method of "Pulse Width Modulation (PWM)"[15].

## VI. CONCLUSION

This paper presents an architecture for analog to digital converter that is based on concepts of "Pulse Width Modulation (PWM)". This conversion contains an intermediary step which involves conversion to a PWM signal, which can be known as a quantity time conversion. The information about input signal is carried by each PWM states (high or low). There will be a displacement in binary or inverted binary code in output by selecting between low or high state. Sample and Hold Circuit is not required by this architecture and is faster in comparison with other architectures for ADC. Such ADC offers an advantage of extending multiple sampling simultaneously.

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