International Journal of Psychosocial Rehabilitation, Vol. 24, Issue 07, 2020
ISSN: 1475-7192

BUILT-IN COARSE GAIN CALIBRATION, RESOLUTION TWO-STEP TDC CMOS BY PULSE-SHRINKING FINE STAGE

K.VANISREE, MUDE SREENIVASULA,D.NARESH,Y.
Associate Professor, Professor, Assistant professor,
Department of ECE,
Samskruti College of Engineering and Technology, Ghatkesar.

Abstract:
This paper suggests a computerized converter (TDC) opportunity that concurrently meets a wide variety of knowledge and fine-time targets. In the second step, the suggested TDC uses beat contracting (PS) plot for a fine target and two-advance (TS) engineering for a wider range. By utilizing an implied counterbalance beat and a balance beat width identification plans, the proposed PS TDC forestalls an undesirable non-uniform contracting rate problem in the conventional PS TDCs. The suggested TS architecture obtains nonlinearity with a few techniques, introducing an implied coarse raise adjustment scheme, owing to the sign spread and extension fraud between coarse and fine phases. In a 0.18-µm normal CMOS invention, the replication results of the TDC modified display 2.0-ps objectives and 16-piece go relative to 130-ns input period interim of 0.08-mm2 area. It runs at 3.3 MS/s with a 1.8-V supply of 18.0 maws and achieves a single-shot precision of 1.44-ps.

Index Terms-Built-in coordination, beat contracting (PS), transition time-to-advanced, two-stage (TS).

1. INTRODUCTION

BASED on the recent improvement in CMOS process scaling, due to high-speed transistors and decreased supply voltage, time resolution is becoming more and more superior to voltage resolution [1], [2]. For different uses, such as ADPLLs, space science software, jitter calculations, and so on, a time-to-digital converter (TDC) has recently been used. With the recent increase in TDC efficiency, in particular, it is also used in high-precision flight time.

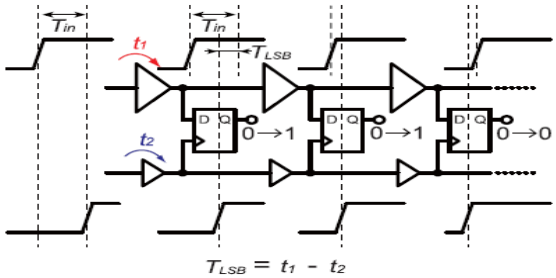


Fig. 1. Simplified schematic of a typical Venire TDC.

Applications for testing, such as the laser range finder [3] and mass spectrometry [4]. It is often used in imaging systems for fluorescence lifetime [5]. Fine time resolution and broad dynamic range are required at the same time in these applications, which are the key target applications of this paper [6]. Because the overall efficiency of the measurement is calculated by the TDC, a few PHS time resolutions with low jitter at multiple MS/s samplingratesare always needed. Several time conversion techniques which realize sub-gate-delay resolution have been proposed in terms of fine resolution. Thanks to the versatility of its architecture principle, the Venire TDC is commonly adopted [6]-[9]. As highlighted in Fig. 1, two separate delay lines that are sometimes introduced as ring delay lines to save area are required by a standard Venire TDC. Two lines have separate delay stages, e.g. t1 and t2 (t2 < t1), so the initial time period Tin progressively shrinks between two rising transitions before the change in the lower delay line meets up with that in the upper one. We may realize fine time resolution by adjusting the delay distinction TLSB = t1-t2. This design, though, includes two separate delay lines where there is an inherent mismatch between them.

The pulse-shrinking (PS) TDC, on the other side, is seen in Fig. Instead of the two separate delay lines [10], [11], 2, which is also a form of Venire TDCs, uses the delay gap between growing and dropping buffer transitions.

The buffer is purposely built to provide varying delays of rise and fall, e.g. trend t f (t f <try), and hence the incoming pulse diameter shrinks TLSB = try−t f by propagating until it disappears across each buffer level. Unlike TDCs from Venire,

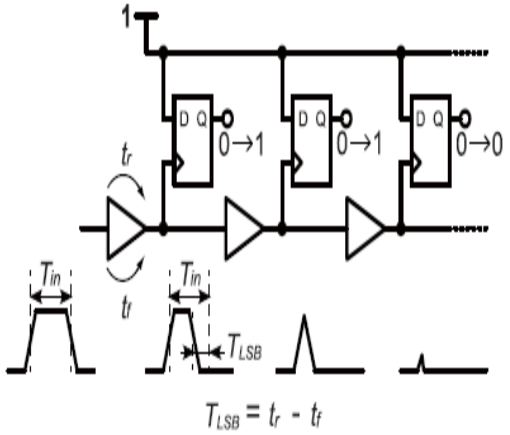


Fig. 2. Simplified schematic of a typical PS TDC.

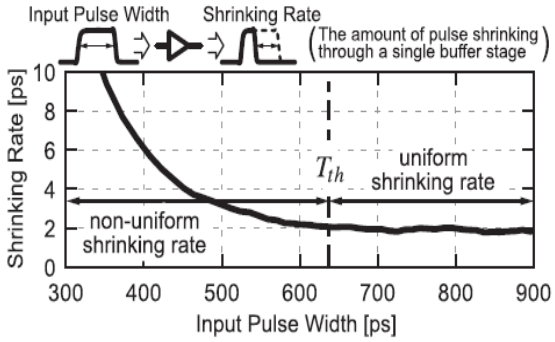


Fig. 3. Simulated PS rate versus input pulse width.

So far, the TDCs' design has centered on fine time resolution. For a broad dynamic spectrum, however,

It could just become unattractive. A Venire TDC with an N-bit and time resolution, for instance, uses 2N delay elements and has a dynamic spectrum of 2N. The dynamic spectrum is therefore halved if the time resolution is cut by half. The TDC then needs additional 2N delay components to retain the same dynamic range, which increase region occupancy, slow down conversion rate, and increase jitter accumulation as N grows greater. One of the basic ideas for expanding the dynamic spectrum while resisting a rise is a looped TDC architecture [13]. A loop counter calculates the amount of cycles the start signal on the loop rotates before the stop signal catches up. From the counter performance and the thermometer code given by the DFFs, the total conversion outcome can be determined. The input spectrum can be reached in an optimal scenario.

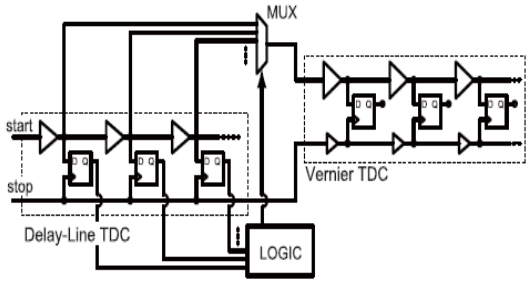


Fig. 4. Schematic of a typical TS TDC [14], [15].

In this article, we employ a sub-gate-delay resolution PS architecture as the fine TDC of the TS architecture in order to obtain a fine resolution and broad range at the same time, and suggest some strategies to solve the problems addressed so far in the traditional PS and TS TDCs. A novel pulse injection with a built-in offset pulse is used in the recommended PS TDC and often leaves the propagating pulse larger than the offset one. Then, when detecting the initial offset pulse width that is set wider than the threshold Th, the PS TDC completes the conversion phase to prevent the non-uniform PS rate problem, as seen in Fig. 3 of [11]. The PS TDC realizes a fine time resolution dependent on this scheme, prevents excessive jitter accumulation, and saves conversion time and resource usage, thus inheriting the benefits of the traditional PS TDC

architecture. The proposed TS TDC eliminates the usage of the inter-stage multiplexer and overcomes the problem of resolution mismatch with an optimized coarse gain calibration mechanism such that a broad dynamic range and a fine time resolution are realized at the same time by the proposed TS TDC.

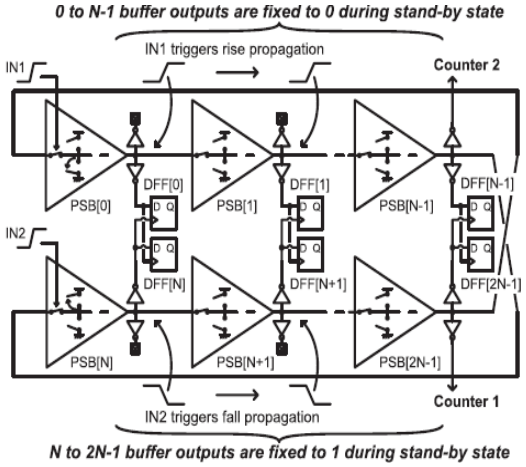


Fig. 5. Block diagram of the proposed fine TDC based on the PSBR.

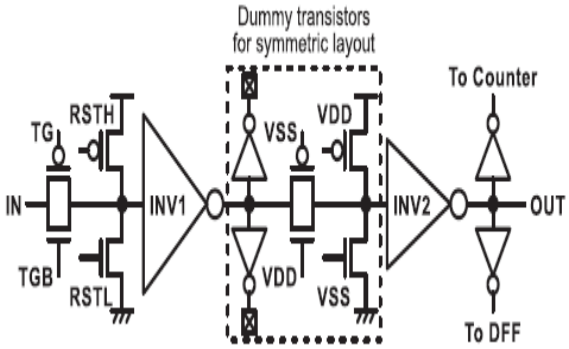


Fig. 6. Detailed schematic of the PSB.

The remainder of this article is structured as follows. The design and the conversion concept of the proposed TDC are defined in Section II. The circuit implementation and post-layout simulation outcomes of the proposed TDC are discussed in Section III. Then, this paper ends with Section IV.

2. Two-step TDC ARCHITECTURE PROPOSED

A. Pulse-Shrinking TDC Fine-Stage

The PS buffering (PSBR) based block diagram of the fine-stage TDC is shown in Fig. 5. The 2N-stage PS buffers are primarily composed of (PSBs). The Kth PSB output (k = 0, N − 1) is linked to theKth DFF data input and the (N + k) Th DFF clock input, while the (N + k) Th PSB output is linked to both the (N + k) Th and Kth DFF data on the opposite side of the ring. In

addition, the outputs of PSBs (N-1) and (2N-1) are connected to counters beyond the centre of the PSBR.

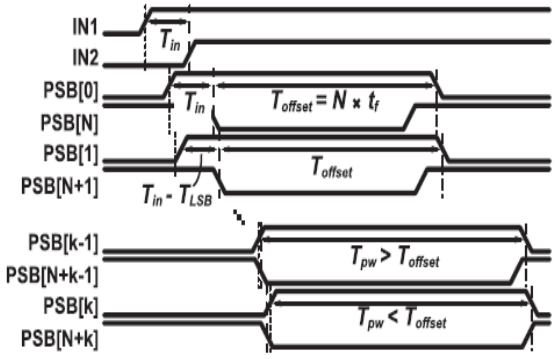


Fig. 7. Timing diagram of the PS TDC.

Because the PSB performance on the opposite side of the ring is expected to have an opposite signal shift,The Kth PSB output increases later than the dropping edge of the (N + k)this output as the propagating pulse width T pw becomes equivalent to the initial built-in offset pulse width Offset, then the Kth DFF adjusts its output from 0 to 1, as shown in Fig. 8. This TDC identifies the initial built-in Offset by defining this DFF output transition, and activates the completion warning. Therefore, even though T offset fluctuates due to method variance, Offset's absolute value has no effect on the process of conversion. Since T offset is selected to satisfy Offset>Th in Fig. by default. 3, the non-uniform shrinking rate concern would not impact the suggested TDC.

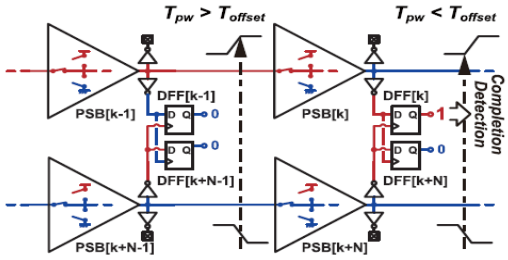


Fig. 8. Detailed PSBR schematic at the moment of the completion of conversion.

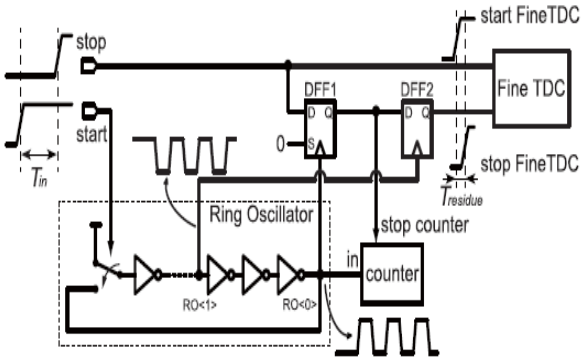


Fig. 9. Block diagram of the proposed TS TDC.

B. Architecture of the Two-Step TDC

The block diagram of the TS TDC architecture suggested is shown in Fig. 9. A ring oscillator containing a counter

The PS TDC functions as the coarse TDC, and the PS TDC functions as the fine stage in Section II-A. Unlike traditional TS TDCs, the two TDCs are coupled by two DFFs in the proposed TDC to prevent the non-idealities of the inter-stage multiplexers. The second DFF however, DFF2 in Fig. 9, linked to the fine TDC seems to be redundant, because of asynchronous timing between RO0 and the input stop signal, it alleviates a met stability problem in DFF1. In addition, the two DFFs have another function to perform in the proposed built-in tuning process alluded to in Section II-C.

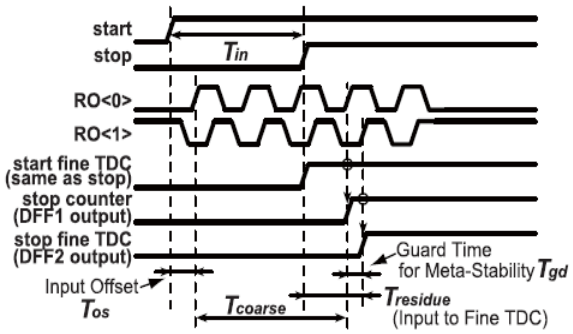


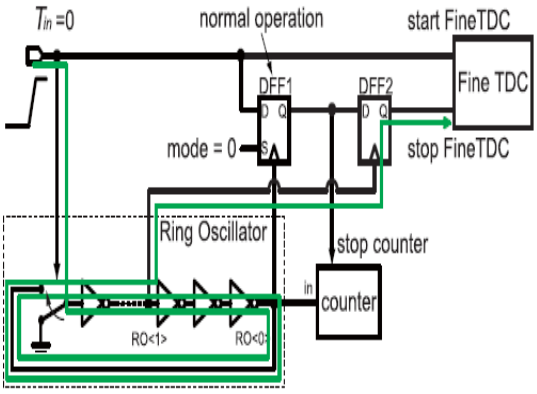
Fig. 10. Timing diagram of the proposed TS TDC.

It acts as a time guard to prevent met stability. The period residue induced by this roundup, Residue, in Fig., by the above-mentioned method. 10, is injected for a fine transfer into the second stage TDC. The overall input time period is ultimately resolved according to

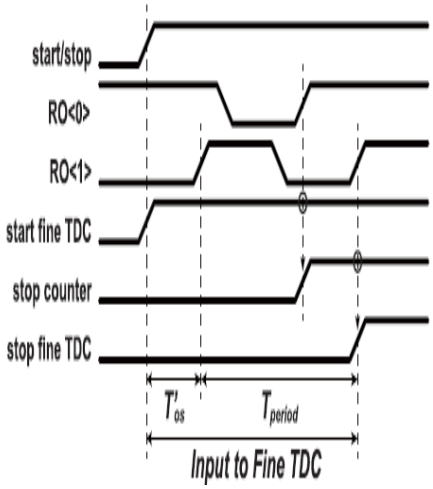
$$T_{\text{in}} = T_{\text{os}} + T_{\text{coarse}} + T_{\text{gd}} - T_{\text{residue}} \qquad (1)$$

C. Built-In Coarse Gain Calibration

The calibration scheme suggested is based on the mechanism of built-in calculation. By calculating a time interval corresponding to 1 LSB of the coarse TDC with the fine TDC, the necessary ratio of the resolutions can be obtained. Two separate paths are switched in the calibration phase by using DFF1's S (Fixed) data, which is used to set its output Q to big, as seen in Figs. Eleven and 12. First of all, the input of the first-stage inverter is set to GND during calibration mode until the process begins. When DFF1 is in regular mode with an input of 0 to the S-port, as seen in Fig. 11(a), given Tin = 0, after one cycle of coarse oscillation period, the fine TDC is stopped plus the input offset time T so, as summarized in the timing diagram.



(a)



(b)

3. PROTOTYPE IMPLEMENTATION AND SIMULATION

In a 0.18-µm normal CMOS technology, the suggested TS TDC is introduced, as seen in Fig. Thirteen, and its, and its,
With post-layout emulation, efficiency is checked.

A. TDC Fine-Stage

The lower portion of Fig. 13 indicates the PSB positioning in the fine TDC of the PSBR core, which has 32 PSB phases. Kth The

The PSBs (k = 0, . . ., 15) and (k + 16) are located next to each other to relax the DFF relations shown in Fig. 5, and PSBsare arranged so that inter-PSB link wire lengths are equivalent. The transistor size and current consumption of PSB inverters have to be carefully selected since it is important to recognize the effect of jitter accumulation and process variance. On the basis of the jitter analysis in eel, we calculated the transistor sizes of the PSB

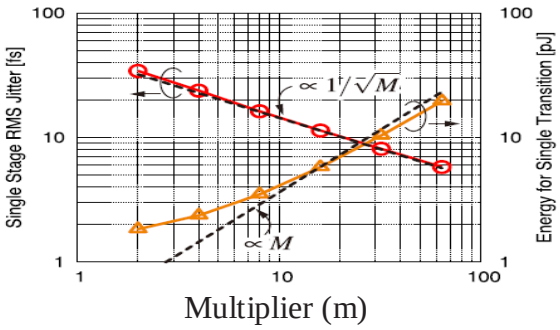


Fig. Fig. Oh. 14. Schematic-level simulation benefits from a single-stage PSB jitter and energy for a single raise transformation based on the width of the transistor. Wombs = 8.32 = M am and Winos = 4.00 = M am for INV1 in PSB. Wombs = 8.00 M am and Winos = 4.00 M am for INV2. The rams jitter is measured with thermal noise simulations of 1024 Monte Carlo times. The initial noise on the output capacitor [17], the jitter, is created by the white noise generated by the resistance of the channel.

$$\sigma_{t_{dP}} \approx \sqrt{\frac{4kT\gamma_P t_{dP}}{I_P(V_{DD} - V_{tP})}} \qquad (3)$$

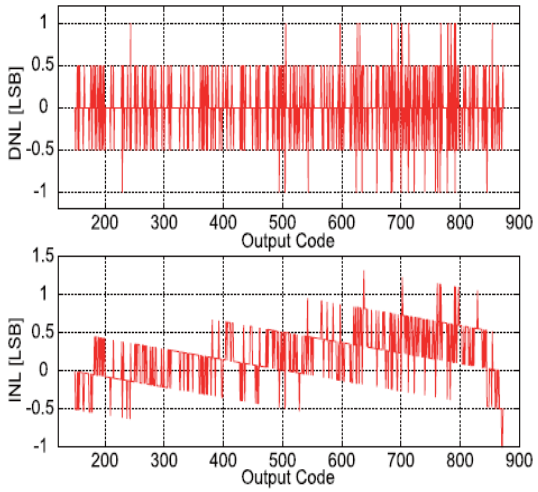


Fig. 16. Simulation results of DNL and INL of the fine-stage PS TDC.

B. Two-Step TDC

The transistor sizes of the coarse TDC ring oscillator, which has 15 inverter stages, are also calculated on the basis of the jitter analysis in [17]. As shown in Fig. 17, with schematic-level simulation by sweeping the transistor distance, we have checked the patterns of jitter and energy for a single increase transformation for the coarse stage ring oscillator. With the simulation effects at M = 16, the black dotted lines are standardized. Jitter and energy are obviously in

proportion to 1/M and M, respectively, as predicted, since basic inverters are used by the coarse staggering oscillator. Since the coarse stage covers a spectrum of up to 7 bits in our TS TDC, with the limit

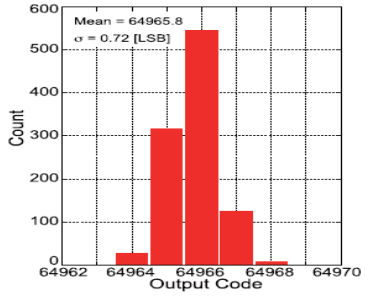


Fig. 17 Post-layout simulation result of single-shot code distribution of the TS TDC.

Get the conversion done. In this scenario, in the fine stage, 47.8 percent of the overall power is absorbed, while the remainder is in the coarse stage. In Fig., simulated DNL and INL are plotted. 19. 19. The simulation range is at the centre of the input time interval range, where the INL becomes its maximum because of the slightly actuate form induced by the calibration error of the transfer characteristic of the TDC. The comprehensive transition function of this spectrum is also seen in Fig. Eighteen. The full DNL and INL of −1.0/+1.0 and −2.0/+1.0 LSB was obtained by the TDC, respectively.

Ref.	TCAS'14 [6]	JSSC'10 [7]	MEJ'15 [9]	JSSC'12 [18]	JSSC'13 [19]	JSSC'14 [20]	ASSCC'16 [11]	This work
Architecture	3D Vernier	2D Vernier	Vernier Sub-Ranging	Cyclic	Two-Step (Time Amp.)	Pipeline	Pulse Shrinking (PS)	Two-Step PS
Tech. [nm] (Meas. / Sim.)	130 Meas.	65 Meas.	130 Meas.	130 Meas.	65 Meas.	65 Meas.	180 Meas.	180 Sim.**
Resol. [ps]	7	4.8	5	1.25	3.75	1.12	1.8	2.00
Precision rms [ps] (T_R at the meas. or sim.)	20.8 (@1.4 ns)	-	2.05 (0~300 ps)	~1.25* (@40 ps)	-	0.77 (@~348 ps*)	2.16 (@860 ps)	1.44 (@129.5 ns)
Rate [MS/s]	25	50	20	50	200	250	4.4	3.3
Range [bit]	11	7	6	8	7	9	9	16
DNL [LSB]	0.8	1	0.63	0.7	0.9	0.6	1.2	1.5
INL [LSB]	1.5	3.3	1.47	3.0	2.3	1.7	8.7	4.2
Power [mW]	0.33(@1MHz)	1.7	1.15	4.3	3.6	15.4	3.4	18.0
Area [mm^2]	0.28	0.02	0.7	0.07	0.02	0.14	0.07	0.08
FoM [pJ/conv.-step]	0.40	1.14	1.96	1.34	0.46	0.32	14.6	0.43

* calculated from the figure of the measurement result. ** Monte-Carlo simulation result that leads to the worst FoM.

Compared with some recently recorded sub-gate-delay resolution TDCs in Table I, the efficiency of the proposed TS TDC is compared. The figure of merit (Form), which is commonly used for TDC comparison, is used to render a reasonable comparison.

[6], [19] and [20] have been adopted. The Form is known as

$$\text{FoM} = \frac{\text{Power}}{(2^{N_{\text{linear}}} \times f_s)} \qquad (6)$$

Where the effective number of linear bits (*L*inear) is given by

$$N_{\text{linear}} = \text{Range [bit]} - \log_2(\text{INL} + 1). \qquad (7)$$

The Monte Carlo simulation results are listed for the proposed TDC with the worst case of M. The proposed TDC, utilizing advanced 0.18-μm CMOS technology, realizes ultra-wide range and fine time resolution at the same time thus achieving competitive Form.

4. CONCLUSION

This paper introduced a broad variety of inputs and TDC fine-time resolution mixing architectures of PS and TS.

A novel pulse injection with a built-in offset pulse and an offset pulse width detection systems prevents an unacceptable non-uniformity of pulse shrinking rate in the fine-stage PS TDC in traditional PS TDCs. This leads to fine resolution and low-jitter time-to-digital transfer, thus inheriting the benefits of the PS TDC system, such as small-area deployment. In order to extend the input spectrum, the proposed TS design is added to the PS TDC. The suggested TS TDC integrating a built-in coarse gain calibration system overcomes the functional challenge due to the non-ideality of the direction of inter-stage signal propagation and the gain discrepancy between the two levels. The detailed findings of the simulation revealed that 16-bit large dynamic range and 2.0-ps fine resolution were realized at the same time by the proposed TDC. A competitive Fromm is achieved,
In contrast with the recently published sub-gate-delay resolution TDCs, utilizing mature 0.18-μm technology.

REFERENCES

[1] R. B. Staszewski et al., "All-digital TX frequency synthesizer anddiscrete-time receiver for Bluetooth radio in 130-nm CMOS," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[2] K. Asada, T. Nakura, T. Iizuka, and M. Ikeda, "Time-domain approach for analog circuits in deep sub-micron LSI," IEICE Electron. Express, vol. 15, no. 6, pp. 1–21, 2018.

[3] P. Palojärvi, K. Määttä, and J. Kostamovaara, "Integrated time-of-flight laser radar," IEEE Trans. Instrum. Meas., vol. 46, no. 4, pp. 996–999,
Aug. 1997.

[4] K. Sano et al., "Design and high-speed tests of a single-flux-quantum time-to-digital converter for time-of-flight mass spectrometry," in Proc. IEEE 14th Int. Superconductive Electron. Conf. (ISEC), Jul. 2013, pp. 1–3.

[5] M.-W. Seo et al., "A 10 ps time-resolution CMOS image sensor withtwo-tap true-CDS lock-in pixels for fluorescence lifetime imaging," IEEE J. Solid-State Circuits, vol. 51, no. 1, pp. 141–154, Jan. 2016.

[6] Y. Kim and T. W. Kim, "An 11 b 7 ps resolution two-step time-to digital converter with 3-D Vernier space," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 8, pp. 2326–2336, Aug. 2014.

[7] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," IEEE J. Solid-State Circuits, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.

[8] B. Markovic, S. Tisa, F. A. Villa, A. Tosi, and F. Zappa, "A high-linearity,17 ps precision time-to-digital converter based on a single-stage Vernier delay loop fine interpolation," IEEE Trans. Circuits Syst. I, Reg. Papers,
vol. 60, no. 3, pp. 557–569, Mar. 2013.

[9] C.-T. Ko, K.-P. Pun, and A. Gothenberg, "A 5-ps Vernier sub-ranging time-to-digital converter with DNL calibration," Microelectron. J., vol. 46, no. 12, pp. 1469–1480, Dec. 2015.

[10] C.-C. Chen, S.-H. Lin, and C.-S. Hwang, "An area-efficient CMOS timeto- digital converter based on a pulse-shrinking scheme," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 3, pp. 163–167, Mar. 2014.

[11] T. Iizuka, T. Koga, T. Nakura, and K. Asada, "A fine-resolution pulse shrinking time-to-digital converter with completion detection utilizing built-in offset pulse," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Nov. 2016, pp. 313–316.

[12] P. Chen, S.-I. Liu, and J. Wu, "A CMOS pulse-shrinking delay element for time interval measurement," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 9, pp. 954–958, Sep. 2000.

[13] J.-P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1286–1296, Jun. 2006.

[14] V. Ramakrishnan and P. T. Balsara, "A wide-range, high-resolution,compact, CMOS time to digital converter," in Proc. 19th Int. Conf. VLSI Design (VLSID), Jan. 2006, pp. 197–202.

[15] S. Henzler, Time-to-Digital Converters. Amsterdam, The Netherlands: Springer, 2010.